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INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				APPLICANTS Teruo TAKIZAWA et al.			
				FILING DATE February 23, 2001			
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	
DA		JP 5-235335	09/10/1993	Japan	—	—	
		JP 11-162916 A	06/18/1999	Japan	—	—	
		JP 7-202178 A	08/04/1995	Japan	—	—	
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DA		WO 94/14198 A	06/23/1994	WIPO	—	—	
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
DA		Hwang et al., NOVEL POLYSILICON/TiN STACKED-GATE STRUCTURE FOR FULLY-DEPLETED SOI/CMOS (1992 IEEE)					
DA		King et al., A POLYCRYSTALLINE-Si _{1-x} Ge _x -GATE CMOS TECHNOLOGY (1990 IEEE)					
EXAMINER				DATE CONSIDERED			
				1-25-02			
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							